The rejection states in relevant part:

> Thus, figure 1D *(Austin)* shows all limitations of the claim *(claim 10)* except for the pair of MOSFETs is a dual gated MOSFET. However, Chung teaches in figure 1 a MOS transistor comprising a single drain, a single source and plurality of gates. This MOSFET having a function as plurality of transistors connected in parallel. The advantage of Chung's MOSFET is the chip area can be reduced in device fabrication. Therefore, it would have been obvious to one having ordinary skill in the art to make Austin's pair MOSFET (153 and 154) as a transistor having a single drain, single source, and two gates (dual gated MOSFET) for the purpose of saving space. (Italicized parentheticals added.)

As discussed in previous Office Actions and responses to these Office Actions, the term dual gated MOSFET does not refer to any one type of MOSFET using a dual gate configuration. Concurrently, there is also no conventional circuit representation for a dual gated MOSFET, nor a circuit representation for each particular configuration for the dual gated MOSFET. The use of dual gated MOSFET must therefore be defined in some manner by the reference employing the dual gated MOSFET.

As noted in the Office Action mailed 8 February 2001, the symbol used in the drawings in conjunction with the specification defines the dual gated MOSFET of the instant invention as a dual gated MOSFET having two gates on opposite sides of a body region.

In contrast, Chung relates to a multiple gated MOSFET with all the gates on one side of the MOSFET symbolized by the circuit representation of Fig. 4. Clearly, a dual gated MOSFET with gates on both sides of a body region is distinctly different from a multiple gated MOSFET with gates on one side of a body region. This difference is further illustrated by the circuit representations used in Chung as compared to the circuit representation defining the dual gated MOSFET of the instant invention. Thus, since Chung does not teach or suggest the dual gated MOSFET as defined in the instant invention, Applicant submits that the combination of Austin with Chung does not teach or suggest all the elements as recited in claim 10.

Independent claims 17, 23, 29, 32, 33, 37, 44, and 45 recite similar elements as claim 10 and are patentable over Austin in view of Chung for the reasons stated above plus the elements of the claims. Claims 11 and 13-16, claims 20-22, claims 24 and 26-27, claims 30-31, claims 34-36, claim 38 are dependent on claims 10, 17, 23, 29, 33, and 37, respectively, and are patentable over Austin in view of Chung for the reasons stated above plus the elements of the claims.

Applicant respectfully requests withdrawal of these rejections to claims 10, 11, 13-18, 20-24, 26-27, 29-38, 44 and 45, and reconsideration and allowance of these claims.

Second §103 Rejection of the Claims

Claims 28 and 40-43 were rejected under 35 USC § 103(a) as being unpatentable over Kaneko et al. (US 6,069,828) (previous cited) in view of Austin (US 5,982,690) (previous cited) and Chung (US 5,442,209) (previous cited).

Applicant respectfully traverses these grounds for rejection for the following reasons.

Applicant does not admit that the Austin patent is prior art to the present invention and reserves the right to swear behind this patent at a later date. Nevertheless, Applicant also respectfully submits that Kaneko et al. (hereafter Kaneko) in view of the Austin patent is distinguishable from the present invention.

This Office Action rejection relies on Austin and Chung regarding a sense amplifier having a dual gated MOSFET. Thus, Kaneko does not cure the deficiencies in the Austin and Chung combined references. Since independent claims 23 and 40 recite similar elements as claim 10, they are patentable over Austin in view of Chung for the reasons stated above plus the elements of the claims. Claim 28 and claims 40-43 are dependent on claims 23 and 40, respectively, and are patentable over Kaneko in view Austin and Chung for the reasons stated above plus the elements of the claims.

Applicant respectfully requests withdrawal of these rejections to claims 28, and 40-43, and reconsideration and allowance of these claims.

Comment Regarding Rejections Based on "Design Choice"

The Office Action rejection claims 15-16, 21-22, 26-27, 30-31, and 41-42 based in part as "an obvious design expedient dependent upon particular environment of use to ensure optimum performance." The mere fact that design choices are made in an innovation does not make the design choice obvious. One would expect an obvious design choice to be selected from a relatively known set of parameters, finite or infinite in number, but nonetheless from a known set of possibilities. A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie, 559* F.2d 618, 195 USPQ 6 (CCPA 1977). *See MPEP §2144.05*

Therefore, Applicant submits that the Office Action statement "an obvious design expedient dependent upon particular environment of use to ensure optimum performance," without some reference regarding the parameters does not provide a specific reason for the rejections of claims 15-16, 21-22, 26-27, 30-31, and 41-42, and therefore the Office Action has not made a prima facie case for obviousness. Further, Applicant respectfully requests that a reference, pursuant to MPEP §2144.03, which describes these parameters related to a sense amplifier using a dual gate MOSFET.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612 371-2157) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2157

Date 22 July 2002 By David R. Cochran

David R. Cochran
Reg. No. 46,632

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner of Patents, Washington, D.C. 20231, on this 22nd day of July, 2002.

Name Amy Moriarty Signature Amy Moriarty